



ASSOCIATION CONNECTING  
ELECTRONICS INDUSTRIES®

---

# IPC-6018A

## Microwave End Product Board Inspection and Test

### **IPC-6018A**

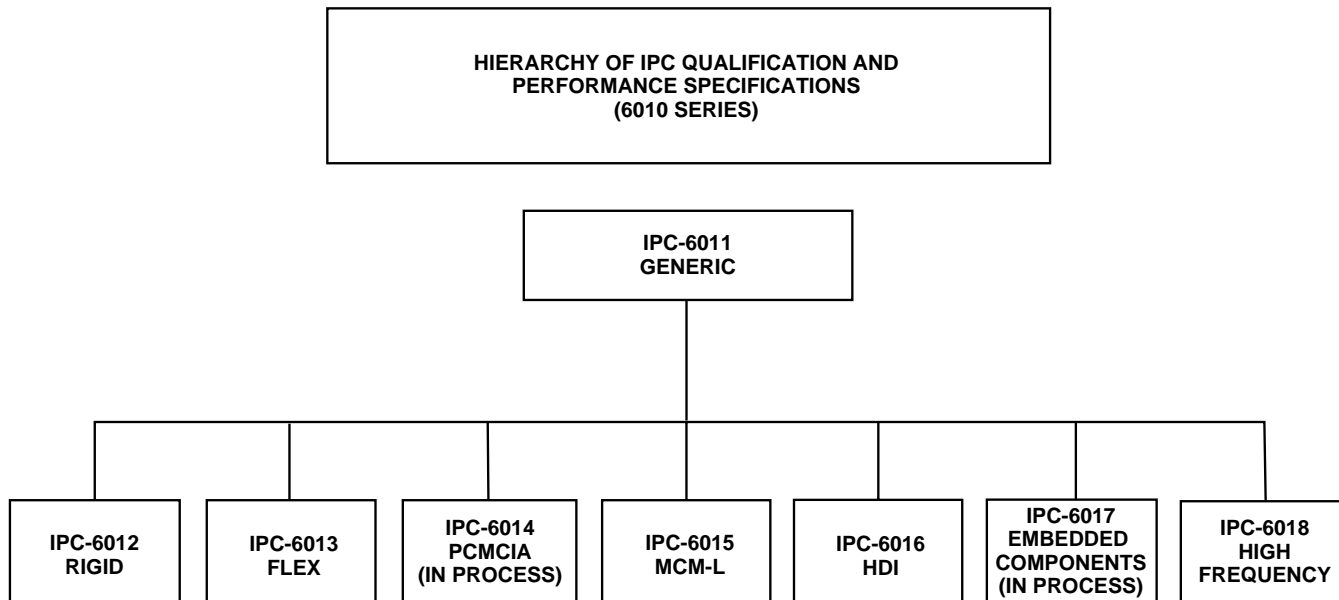
January 2002

A standard developed by IPC

Supersedes IPC-6018  
January 1998

---

2215 Sanders Road, Northbrook, IL 60062-6135  
Tel. 847.509.9700 Fax 847.509.9798  
[www.ipc.org](http://www.ipc.org)



## FOREWORD

This specification is intended to provide information on the detailed performance criteria of high frequency printed boards. It supersedes IPC-6018 and was developed as a revision to that document. The information contained herein is also intended to supplement the generic requirements identified in IPC-6011. When used together, these documents should lead both manufacturer and customer to consistent terms of acceptability.

IPC's documentation strategy is to provide distinct documents that focus on specific aspects of electronic packaging issues. In this regard, document sets are used to provide the total information related to a particular electronic packaging topic. A document set is identified by a four digit number that ends in zero (0) (i.e., IPC-6010).

Included in the set is the generic information, which is contained in the first document of the set. The generic specification is supplemented by one or multiple performance documents, each of which provide a specific focus on one aspect of the topic or the technology selected.

Failure to have all information available prior to building a board may result in a conflict in terms of acceptability.

As technology changes, a performance specification will be updated, or new focus specifications will be added to the document set. IPC invites input on the effectiveness of the documentation and encourages user response through completion of "Suggestions for Improvement" forms located at the end of each document.

# Table of Contents

<b>1 SCOPE</b> .....	1	3.5.1 Hole Size, Slots and Hole Pattern Accuracy .....	7
1.1 Scope .....	1	3.5.2 Annular Ring and Breakout (Internal) .....	8
1.2 Purpose .....	1	3.5.3 Annular Ring (External) .....	8
1.3 Performance Classification and Types .....	1	3.5.4 Bow and Twist .....	8
1.3.1 Classification .....	1	3.6 Conductor Definition .....	8
1.3.2 Board Type .....	1	3.6.1 Undercutting .....	9
1.3.3 Selection for Procurement .....	1	3.6.2 Conductor Width and Spacing .....	9
1.3.4 Material, Plating Process and Final Finish .....	1	3.6.3 Conductive Surfaces .....	10
1.4 Master Drawing .....	2	3.7 Structural Integrity .....	11
<b>2 APPLICABLE DOCUMENTS</b> .....	2	3.7.1 Thermal Stress Testing .....	11
2.1 IPC .....	2	3.7.2 Requirements for Microsectioned Coupons or Production Boards .....	12
2.2 American Society for Testing and Materials .....	3	3.8 Other Tests .....	16
2.3 Society of Automotive Engineers .....	3	3.8.1 Metal Core (Horizontal Microsection) .....	16
<b>3 REQUIREMENTS</b> .....	3	3.8.2 Rework Simulation .....	16
3.1 Terms and Definitions .....	3	3.8.3 Bond Strength, Unsupported Component Hole Land .....	16
3.2 General .....	3	3.9 Solder Resist (Solder Mask) Requirements on Non-PTFE Laminates .....	16
3.2.1 Master Drawing .....	3	3.9.1 Solder Resist Coverage .....	16
3.3 Materials Used in this Specification .....	3	3.9.2 Solder Resist Cure and Adhesion .....	17
3.3.1 Laminates and Bonding Material for Multilayer or Mixed Dielectric Boards .....	3	3.9.3 Solder Resist Thickness .....	17
3.3.2 External Bonding Materials .....	4	3.10 Circuitry .....	17
3.3.3 Other Dielectric Materials .....	4	3.10.1 Circuitry Continuity (Qualification) .....	17
3.3.4 Metal Foils .....	4	3.10.2 Circuitry Continuity (Production) .....	17
3.3.5 Metal Core/Backed .....	4	3.10.3 Circuit Shorts .....	17
3.3.6 Metallic Platings and Coatings .....	4	3.10.4 Dielectric Withstanding Voltage .....	17
3.3.7 Organic Solderability Preservative (OSP) .....	4	3.10.5 Insulation Resistance .....	18
3.3.8 Polymer Coating (Solder Resist) .....	5	3.10.6 Circuit/Plated-Through Shorts to Metal Substrate .....	18
3.3.9 Fusing Fluids and Fluxes .....	5	3.10.7 Moisture and Insulation Resistance (MIR) .....	18
3.3.10 Marking Inks .....	5	3.10.8 Dielectric Withstanding Voltage After MIR .....	18
3.3.11 Hole Fill Insulation Material .....	5	3.11 Cleanliness .....	18
3.3.12 Heatsink Planes, External .....	5	3.11.1 Cleanliness Prior to Solder Resist Application .....	18
3.4 Visual .....	6	3.11.2 Cleanliness After Solder Resist, Solder, or Alternative Surface Coating Application .....	18
3.4.1 Edges of Microwave Boards .....	6	3.11.3 Cleanliness of Inner Layers After Oxide Treatment Prior to Lamination .....	18
3.4.2 Laminate Imperfections .....	6	3.12 Special Requirements .....	18
3.4.3 Plating and Coating Voids in the Hole .....	6	3.12.1 Outgassing .....	18
3.4.4 Lifted Lands .....	6	3.12.2 Organic Contamination .....	18
3.4.5 Marking .....	6	3.12.3 Fungus Resistance .....	19
3.4.6 Solderability .....	7	3.12.4 Vibration .....	19
3.4.7 Plating Adhesion .....	7	3.12.5 Mechanical Shock .....	19
3.4.8 Edge Board Contact, Junction of Gold Plate to Solder Finish .....	7		
3.4.9 Workmanship .....	7		
3.5 Board Dimensional Requirements .....	7		

3.12.6	Impedance Testing .....	19
3.12.7	Coefficient of Thermal Expansion (CTE) .....	19
3.12.8	Thermal Shock .....	19
3.12.9	Surface Insulation Resistance (As Received) ...	20
3.12.10	Wire Bond Adhesion .....	20
3.12.11	Die Bond Adhesion.....	20
3.13	Repair .....	20
3.13.1	Circuit Repairs .....	20
3.14	Rework .....	20
<b>4</b>	<b>QUALITY ASSURANCE PROVISIONS</b> .....	<b>20</b>
4.1	General .....	20
4.1.1	Qualification .....	20
4.1.2	Sample Test Coupons .....	20
4.2	Acceptance Tests.....	20
4.2.1	C=0 Sampling Plan.....	20
4.2.2	Referee Tests .....	20
4.3	Quality Conformance Testing.....	20
4.3.1	Coupon Selection.....	20
4.3.2	Test Equipment and Inspection Facilities .....	20
4.3.3	Tolerances.....	21
<b>5</b>	<b>PACKAGING</b> .....	<b>26</b>
<b>6</b>	<b>NOTES</b> .....	<b>26</b>
6.1	Ordering Data .....	26
<b>APPENDIX A</b>	.....	<b>27</b>

### Figures

Figure 3-1	Adhesive Band Near Exposed Conductor.....	7
Figure 3-2	Annular Ring Measurement.....	8
Figure 3-3a	Breakout of 90° and 180° .....	8
Figure 3-3b	Conductor Width Reduction.....	8
Figure 3-4	Conductor Edge Definition.....	9
Figure 3-5	Undercut and Growth .....	10

Figure 3-6	Crack Definition .....	14
Figure 3-7	Etchback in Contact with PTFE Layer .....	14
Figure 3-8	Negative Etchback.....	14
Figure 3-9	Metal Core to Plated-Through Hole Spacing ..	15
Figure 3-10	Separations at External Foil .....	19
Figure A-1	Zero Defects Graphic Illustration.....	27

### Tables

Table 1-1	Default Requirements.....	1
Table 3-1	Metal Core Substrate .....	4
Table 3-2	Final Finish, Surface Plating Coating Requirements .....	5
Table 3-3	Plating and Coating Voids Visual Examination....	6
Table 3-4	Edge Board Contact Gap.....	7
Table 3-5	Minimum Annular Ring .....	9
Table 3-6	Percent of Allowable Conductor Width Deviations .....	10
Table 3-7	Percent of Allowable Conductor Space Deviations .....	10
Table 3-8	Critical Conductor Tolerance Requirements for 1/2 Ounce Copper.....	10
Table 3-9	Percent of Allowable Conductor Width Reduction Caused By Pin Holes.....	10
Table 3-10	Percent of Reduction in Dielectric Material Thickness.....	11
Table 3-11	Plated-Through Hole Integrity After Stress .....	13
Table 3-12	Internal Layer Foil Thickness After Processing.....	15
Table 3-13	External Conductor Thickness After Plating .....	15
Table 3-14	Solder Resist Adhesion .....	17
Table 3-15	Dielectric Withstanding Voltages.....	17
Table 3-16	Insulation Resistance .....	18
Table 4-1	Qualification Test Coupons .....	21
Table 4-2	C=0 Sampling Plan (Sample Size for Specific Index Value*) .....	22
Table 4-3	Acceptance Testing and Frequency .....	23
Table 4-4	Quality Conformance Testing .....	26

# Microwave End Product Board Inspection and Test

## 1 SCOPE

**1.1 Scope** This specification covers end product inspection and test of high frequency (microwave) printed boards for microstrip, stripline, mixed dielectric and multilayer stripline applications with or without buried/blind vias, and metal cores.

**1.2 Purpose** The purpose of this specification is to provide requirements for qualification and performance of high frequency (microwave) printed wiring boards.

### 1.3 Performance Classification and Types

**1.3.1 Classification** This specification recognizes that the printed boards will be subject to variations in performance requirements based on end-use. The high frequency printed wiring boards are classified by Performance Class 1, 2, or 3. Performance classes are defined in IPC-6011, Generic Performance Specification for Printed Boards.

**1.3.2 Board Type** This specification will define seven types of high frequency (microwave) boards.

Type 1 — Single Sided

Type 2 — Double Sided

Type 3 — Homogeneous Multilayer Construction

Type 4 — Mixed Dielectric Multilayer

Type 5 — Homogeneous Multilayer with Blind and/or Buried Vias

Type 6 — Mixed Dielectric Multilayer with Blind and/or Buried Vias

Type 7 — Metal Core/Backed Boards

**1.3.3 Selection for Procurement** For procurement purposes, performance class **shall** be specified in the procurement documentation.

The documentation **shall** provide sufficient information to the supplier so that he can fabricate the printed board and ensure that the user receives the desired product. Information that should be included in the procurement documentation is shown in IPC-D-325.

**1.3.3.1 Selection** The procurement documentation should specify the requirements that can be selected within this specification. Refer to Table 1-1 for a listing of default requirements.

### 1.3.4 Material, Plating Process and Final Finish

**1.3.4.1 Laminate Material** Laminate material is identified by numbers and/or letters, classes, types as specified by the appropriate specification listed in the procurement documentation.

Table 1-1 Default Requirements

Category	Default Selection
Performance Class	Class 2
Final Finish	Finish X (Electrodeposited tin-lead, fused or solder coated)
Minimum Starting Foil	1/2 oz. For all internal and external layers except for Type 1 which shall start with one ounce.
Copper foil type	Electrodeposited
Hole Diameter tolerances Plated, components Plated, via only Unplated	(±) 100 µm [3937 µin] (+) 80 µm [3150 µin], (-) no requirement, may be totally or partially plugged (±) 80 µm [3150 µin]
Conductor Width Deviation	Class 2 deviation per para. 3.6.2.1
Conductor Spacing Deviation	Class 2 deviation per para. 3.6.2.2
Marking Ink	Contrasting color, nonconductive
Solder Resist	Not applied if not specified
Solderability Test	Category 2 of J-STD-003
Solder Resist Specified	Class T of IPC-SM-840 if class not specified
Test Voltage Insulation Resistance	500 volts D.C., Class 2 per para. 3.11.7

**1.3.4.2 Plating Process** The copper plating process which is used to provide the main conductor in the holes is identified by one number as follows:

- 1 Acid copper electroplating only
- 2 Pyrophosphate copper electroplating only
- 3 Acid and/or pyrophosphate copper electroplating
- 4 Additive/electroless copper

**1.3.4.3 Final Finish** The final finish can be but is not limited to one of the finishes specified below or a combination of several platings and is dependent on assembly processes and end-use. Thickness, where required, **shall** be specified in the procurement documentation unless listed in Table 3-2. Coating thickness may be exempted in Table 3-2 (i.e., tin-lead plate or solder coating). Designators for final finish are as follows:

S	Solder Coating (Table 3-2)
T	Electrodeposited Tin-Lead, fused) (Table 3-2)
X	Either Type S or T (Table 3-2)
TLU	Electrodeposit Tin-Lead (unfused) (Table 3-2)
G	Gold Electroplate for Edge Board Connectors (Table 3-2)
GS	Gold Electroplate for Areas to be Soldered (Table 3-2)